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Application No.: 08/993,442
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1 1. (Amended) An integrated circuit for image frame rendering and
2 DSP applications, the integrated circuit during operation operating with memory, the
3 integrated circuit comprising:
4 an interface circuit configured to control access to said memory, the
5 interface circuit coupled to said memory;
6 an embedded processor configured to control the integrated circuit, the
7 embedded processor configured to control the interface circuit to receive information
8 therefrom; and
9 an array processor for performing arithmetic calculations, the array
10 processor coupled to the interface circuit to receive information therefrom and connected
11 to the embedded processor via an internal bus;
12 wherein the array processor comprises:
13 a first multiply/accumulator (MAC) unit coupled to a first local
14 memory, the first local memory comprising a first plurality of operands;
15 a second MAC unit coupled to a second local memory, the second
16 local memory comprising a second plurality of operands; and
17 a first shared operand unit coupled to the first MAC unit and the
18 second MAC unit for providing a first shared operand to the first MAC unit for
19 computing a first result in association with the first plurality of operands and to the
20 second MAC unit for computing a second result in association with the second plurality
21 of operands; and
22 wherein the first result and the second result are computed
23 independently of each other; and
24 wherein the array processor further comprises:
25 a second shared operand unit coupled to a third MAC unit and a
26 fourth MAC unit for providing a second shared operand to the third MAC unit and the
27 fourth MAC unit.

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12. (Amended) The integrated circuit according to claim 10
wherein a first instruction stream and a first data stream is maintained for said array
processor, and a second instruction stream and a second data stream is maintained for
said embedded processor.

16. (Amended) The integrated circuit according to claim 10 further
comprising:
a global external bus unit for providing an interface to said integrated
circuit, said global external bus unit coupled to said embedded microprocessor by a
system bus and by a separate dedicated bus.